Abstract

Semiconductor circuit arrangement with trench isolation and fabrication method

An explanation is given of, inter alia, a circuit arrangement containing a trench which penetrates through a charge-storing layer (18) and a doped semiconductor layer (14). The trench simultaneously fulfils a multiplicity of functions, namely an insulating function between adjacent components, the patterning of the charge-storing layer and also the subdivision of doping layers of the semiconductor layer (14).

(Figure 1F)

List of reference symbols

10 to 10c	Semiconductor substrate
12 to 12c	n-doped semiconductor layer
14 to 14c	p-doped semiconductor layer
16 to 16c	Oxide layer
18 to 18c	Floating gate layer
20, 20a	Hard mask layer
30	Cutout
32 to 32c	Trench
40 to 40c	Oxide layer
42 to 42c	Silicon layer
50, 50c	Oxide layer
60, 60b	Cutout
70, 70b	Dielectric layer
72	Control gate layer
74	Arrow
76	Memory circuit
100	Shallow trench
102	Broken line
104, 106	Tunnel oxide at a trench wall
110	Floating gate layer
112, 114	Tunnel oxide at a trench wall
120	Cutout
122	Broken line